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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/240,975	01/29/1999	NAOKI MITSUISHI	HIT-2-010-1-	8031

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EXAMINER	
BRAGDON, REGINALD GLENWOOD	
ART UNIT	**PAPER NUMBER**
2188	35

DATE MAILED: 12/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/240,975	MITSUISHI, NAOKI	
	Examiner	Art Unit	
	Reginald G. Bragdon	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 October 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *31-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *31-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 31-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ugon (4,382,279) in view of Goss ("Single Chip Microcomputer with EPROM Allows Flexible System Design").

As per claim 31, Ugon teaches a microprocessor architecture including an EPROM 101 ("an electrically erasable and programmable ROM capable of storing a program and data"; see figure 2, section M2, column 5, lines 24-26, and column 6, lines 4-5 and 10-11), a ROM section ("a memory"; see figure 2, section M1, and column 6, lines 5-8), and a processing and control unit 104 ("CPU"; see figures 1-2). A program ("first program and data") is stored in sections M1 and M2, where evolving or modifiable data or instructions of this program, including a processing program, are stored in the section M2. The section M1 contains a subprogram "PROG" ("second program") which performs the functions required for writing to the memory. See column 6, lines 63-66.

A main program running includes an instruction, CALL PROG, which calls or jumps to the PROG subroutine ("wherein the program includes an instruction which changes a process of the central processing unit to a process that controls a writing of the ROM based on the write

control program stored in the memory"). See column 7, lines 55-65. The subroutine includes a return instruction, RET, which causes the subroutine to be exited and control returned to the main program ("wherein the write control program includes an instruction which returns the process of the CPU to a process based on the program stored in the ROM after completion of the process that controls the writing of the ROM"). See column 7, lines 34-54, in particular line 54.

With respect to the claimed "write control circuit", Ugon teaches in the abstract circuits for distributing memory write voltages. Also, all EPROMs inherently include circuitry for programming (i.e. writing) to the EPROM.

Furthermore, Ugon teaches an I/O bus input to the processing and control unit 104. Inherently associated with the I/O bus are pins and buffering which constitute an "input and output unit".

Ugon does not teach a second process wherein the CPU re-writes significant portions of the first program stored in the EPROM from outside of the chip via the I/O bus using the write program. It is noted that the claim language broadly sets forth two processes, namely (1) writing significant portions of the first program from outside of the chip using the second program and (2) the first program includes an instruction which changes a process of the central processing unit to a process that controls a writing of the ROM based on the second program and the second program includes an instruction which returns the process of the CPU to a process based on the first program stored in the ROM after completion of the process that controls the writing of the ROM. Process (2) is taught by Ugon as detailed above.

Goss ("Single Chip Microcomputer with EPROM Allows Flexible System Design") teaches that it was known for programs in EPROMs to be significantly reprogrammed from

outside the chip. See page 2, right column, under "In Circuit Reprogrammability". It would have been obvious to one of ordinary skill in the art to have modified Ugon such that the "PROG" subroutine is used to reprogram significant amounts of the "first program" from outside the chip using the I/O bus, as suggested by Goss, since Goss teaches on page 1, left column, last paragraph (spanning to the top of the right column), that this would increase programming flexibility.

As per claim 32, Ugon teaches that the subroutine "PROG" is located in ROM memory. See column 6, lines 5-8 and 63-66.

As per claim 33, the combination of Ugon and Goss does not teach that the "memory" set forth as section M1 is a random access memory (RAM) or that the subroutine "PROG" is copied to the RAM for execution. It would have been obvious to one of ordinary skill in the art to have replaced the memory set forth as section M1 with a RAM and to copy the subroutine "PROG" from the EPROM to the RAM because removing the ROM would reduce the cost of manufacture by having to create only one memory (i.e. EPROM) storing the running program and the subroutine instead of two memories (i.e. EPROM and ROM) each storing different programs while utilizing the RAM (as a "shadow memory") would provide fast access to the subroutine program when modifying the EPROM.

As per claim 34, Ugon teaches a bus D which provides addresses to address registers A1 102 and A2 103 as well as data to data register D 106. Although Ugon does not specify whether this bus is comprised of physically separate address and data busses or a multiplexed address/data bus, Applicant appears to be assuming that the bus is a multiplexed address/data bus. However, a multiplexed address/data bus would meet the claim limitations since at one

point in time the bus is dedicated to providing address data to the address registers A1 102 and/or A2 103 and at another time dedicated to providing data to data register D 106. Therefore, Ugon teaches "a data bus" and "an address bus".

Response to Arguments

3. Applicant's arguments filed 08 October 2003 have been fully considered but they are not persuasive.

Applicant argues, on page 4 of the response, that neither Ugon or Goss suggests performing the writing of significant amounts of a first program from outside of the chip. Applicant further states that this aspect of the claimed invention is not obvious merely because Goss discloses the reprogramming of an EEPROM of a microcomputer from outside the chip. The Examiner disagrees. Goss provides sufficient motivation for one of ordinary skill in the art to combine the Ugon and Goss references. In particular (and as set forth in the action), Goss teaches that it was known for programs (e.g. firmware, user options, or diagnostic routines) in EEROMs to be reprogrammed from outside the chip because this would increase programming flexibility (see Goss at page 1, left column, last paragraph spanning to the top of the right column). This teaching would motivate one of ordinary skill in the art to have modified the teaching of Ugon such that the "PROG" subroutine is used to reprogram significant amounts (wherein the broadest meaning of "significant amounts" is "meaningful amounts") of the program from outside the chip. Therefore the combination of references teaches the claimed invention.

With respect to Applicant's hindsight argument concerning claim 33, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971). It is noted that the system of Goss incorporates a RAM in the microprocessor instead of a ROM. See the microprocessor block diagram on page 2 of Goss.

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

5. Any response to this final action should be mailed to:

Box AF
Commissioner of Patents and Trademarks

Washington, D.C. 20231

All "OFFICIAL" patent application related correspondence transmitted by FAX must be directed to the central FAX number at **(703) 872-9306**:

"INFORMAL" or "DRAFT" FAX communications may be sent to the Examiner at **(703) 746-5693**, only after approval by the Examiner.

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA., Fourth Floor (receptionist).

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reginald G. Bragdon whose telephone number is (703) 305-3823. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and every other Friday from 7:00 AM to 3:30 PM.

The examiner's supervisor, Mano Padmanabhan, can be reached at (703) 306-2903.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Reginald G. Bragdon
Primary Patent Examiner
Art Unit 2188

RGB
December 1, 2003